

Haier eMMC Product family

eMMC 5.1 Specification compatibility

datasheet

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INTRODUCTION

Haier eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard.

eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (V_{DDF} or V_{CC}) whereas 1.8V or 3V dual supply voltage (V_{DD} or V_{CCQ}) is supported for the MMC controller. Haier eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance.

There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Haier NAND flash and achieves optimal performance.

1.0 PRODUCT LIST

[Table 1] Product List

Capacities	eMMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
8 GB	HIKL8G-SSEF	64Gb x 1	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 0.8mm	153FBGA

2.0 KEY FEATURES

- embedded MultiMediaCard Ver. 5.1 compatible.
- Haier eMMC supports features of eMMC5.1 which are defined in JEDEC Standard
 - Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types.
 - Non-supported Features : Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power → V_{CCQ} (1.70V ~ 1.95V) , Memory power → V_{CC} (2.7V ~ 3.6V)

3.0 PACKAGE CONFIGURATIONS

3.1 153 Ball Pin Configuration

[Table 2] 153 Ball Information

Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	V _{CCQ}
M4	V _{CCQ}
N4	V _{CCQ}
P3	V _{CCQ}
P5	V _{CCQ}
E6	V _{CC}
F5	V _{CC}
J10	V _{CC}
K9	V _{CC}
C2	VDDI
M5	CMD
H5	Data Strobe
M6	CLK
J5	V _{SS}
A6	V _{SS}
C4	V _{SS}
E7	V _{SS}
G5	V _{SS}
H10	V _{SS}
K8	V _{SS}
N2	V _{SS}
N5	V _{SS}
P4	V _{SS}
P6	V _{SS}

Ball-side down view

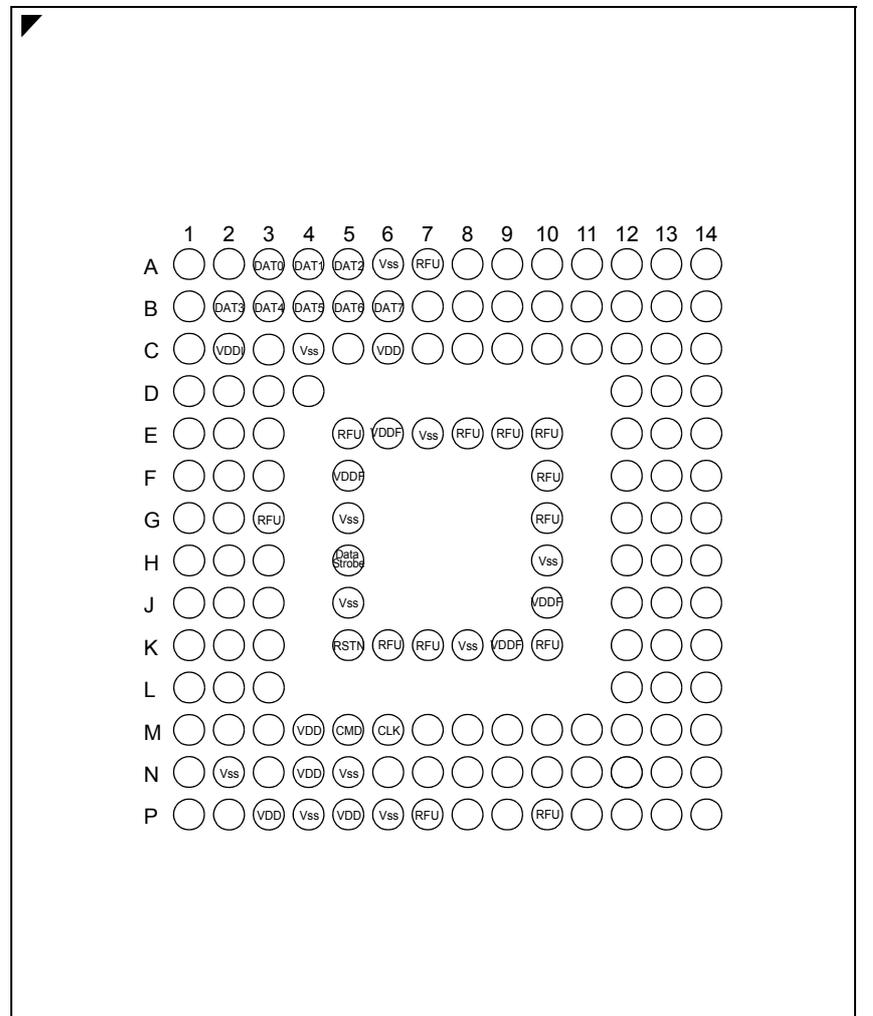


Figure 1. 153-FBGA

- CLK : Clock input
- Data Strobe : Data Strobe is generated from eMMC to host.
In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD : A bidirectional signal used for device initialization and command transfers.
Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7 : Bidirectional data channels. It operates in push-pull mode.
- RST_n : H/W reset signal pin
- V_{CC} : Supply voltage for flash memory
- V_{CCQ} : Supply voltage for memory controller
- VDDi : Internal power node to stabilize regulator output to controller core logics
- V_{SS} : Ground connections
- RFU : Reserved for future use , do not use for any usage

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3.1.3 11.5mm x 13mm x 1.0mm Package Dimension [64GB]

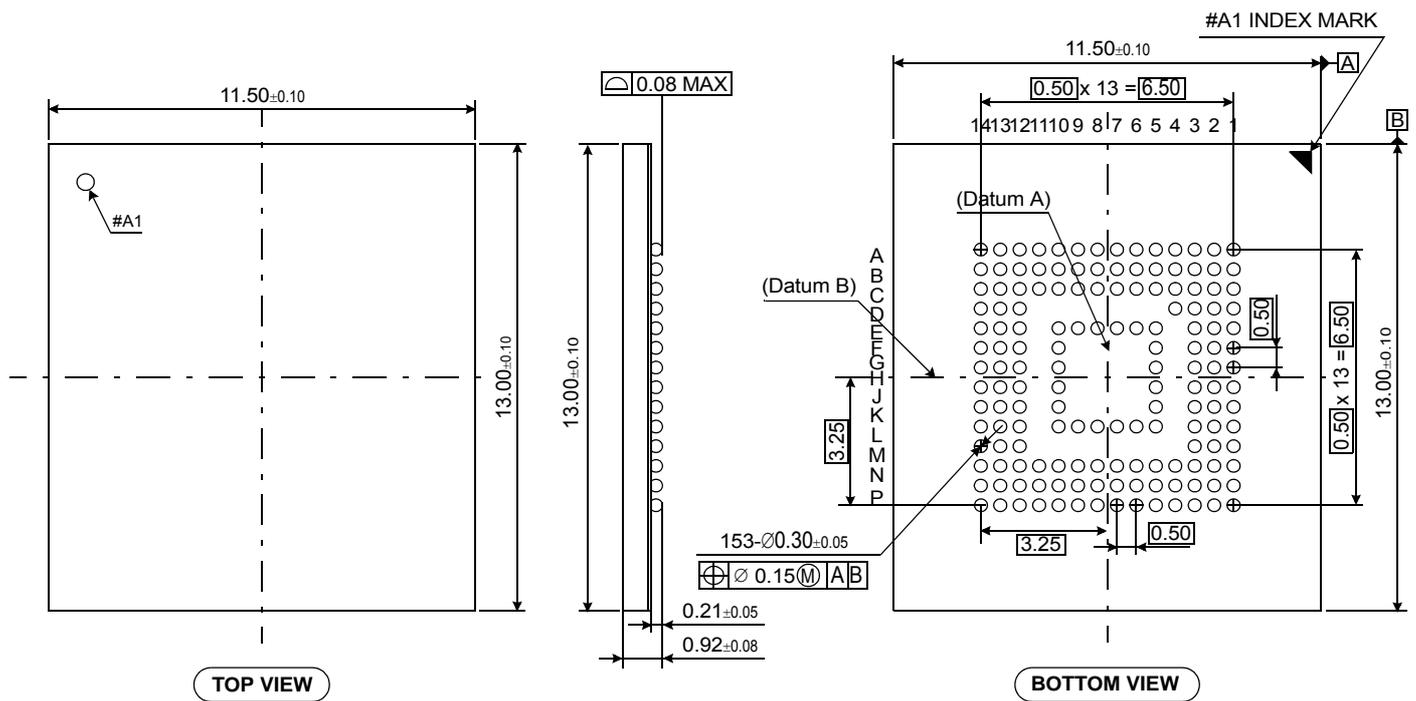


Figure 4. 11.5mm x 13mm x 1.0mm Package Dimension

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3.2 Product Architecture

- eMMC consists of NAND Flash and Controller. V_{CCQ} is for Controller power and V_{CC} is for flash power

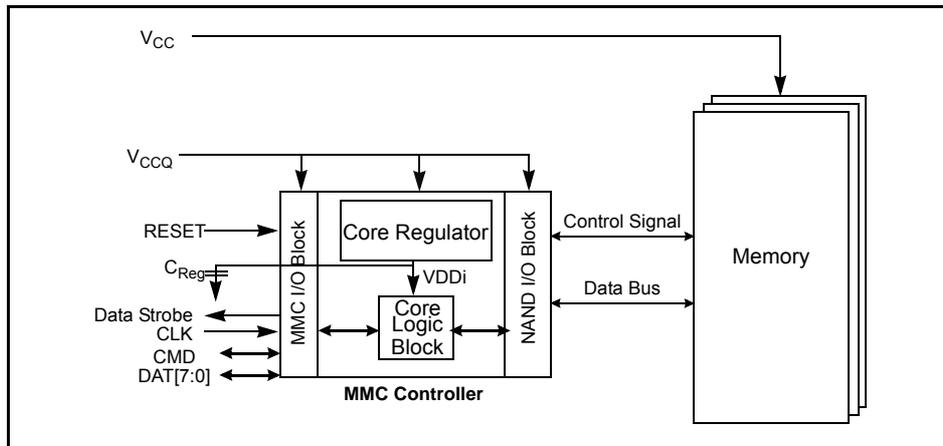


Figure 5. eMMC Block Diagram

4.0 HS400 mode

eMMC5.0 product supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.

HS400 mode supports the following features :

- DDR Data sampling method
- CLK frequency up to 200MHz DDR (up to 400Mbps)
- Only 8-bits bus width available
- Signaling levels of 1.8V
- Six selectable Drive Strength (refer to the table below)

[Table 3] I/O driver strength types

Driver Type	HS200 & HS400 Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0	Default	50Ω	x1	Default Driver Type. Supports up to 200MHz operation.
1	Optional	33Ω	x1.5	Supports up to 200MHz Operation.
2	Optional	66Ω	x0.75	The weakest driver that supports up to 200MHz operation.
3	Optional	100Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design.
4	Optional	40Ω	x1.2	Supports up to 200MHz DDR operation

NOTE:

1) Support of Driver Type-0 is default for HS200 & HS400 Device, while supporting Driver types 1~4 are optional for HS200 & HS400 Device.

[Table 4] Device type values (EXT_CSD register : DEVICE_TYPE [196])

Bit	Device Type	Supportability
7	HS400 Dual Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate eMMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate eMMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed eMMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed eMMC @ 26MHz - at rated device voltage(s)	Support

[Table 5] Extended CSD revisions (EXT_CSD register : EXT_CSD_REV [192])

Value	Timing Interface	EXT_CSD Register Value
255-8	Reserved	-
8	Revision 1.8 (for MMC V5.1)	0x08
7	Revision 1.7 (for MMC V5.0)	-
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-
3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

[Table 6] High speed timing values (EXT_CSD register : HS_TIMING [185])

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

5.0 New eMMC5.1 Features

5.1 Overview

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes
Secure Write Protection	Optional	Yes

5.2 Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.

Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for execution, its state changes to "ready for execution".

The host tracks the state of all queued tasks and may order the execution of any task, marked as "ready for execution", by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command(CMD46/CMD47)

5.2.1 CMD Set Description

[Table 7] CMD Set Description and Details

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming [23] Priority: "0" simple / "1" high [20:16] TASK ID [15:0] number of blocks	QUEUED_TASK_PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data blocks
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data blocks
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK_MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID. When TM op-code = 1h these bits are reserved."

5.2.2 New Response : QSR (Queue Status Register)

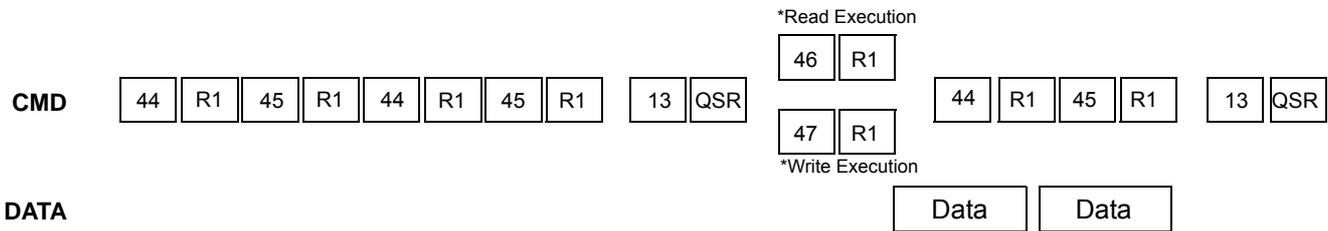
The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit[15]="1"), R1's argument will be the 32-bit Queue Status Register (QSR). Every bit in the QSR represents the task whose ID corresponds to the bit index. If bit QSR[i] = "0", then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR[i] = "1", then the queued task with Task ID i is ready for execution.

5.2.3 Send Status : CMD13

CMD13 for reading the Queue Status Register (QSR) by the host. If bit[15] in CMD13's argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response

5.2.4 Mechanism of CMD Queue operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15]bits to 1 . After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at anytime when the CMD line is not in use



5.2.5 CMD Queue Register description

Configuration and capability structures shall be added to the EXT_CSD register, as described below

[Table 8] CMD Queuing Support (EXT_CSD register : CMDQ_SUPPORT [308])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not

0x0: CMD Queue function is not supported

0x1: CMD Queue function is supported

[Table 9] Command Queue Mode Enable(EXT_CSD register : CMDQ_MODE_EN [15])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							0x00

This field is used by the host enable command queuing

0x0: Queue function is not enabled

0x1: Queue function is enabled

[Table 10] CMD Queuing Depth(EXT_CSD register : CMDQ_DEPTH [307])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved				0x0F			

This field is used to calculate the depth of the queue supported by the device

Bit encoding:

[7:5]: Reserved

[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.

Queue Depth = N+1.

5.3 Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refer to the details as described in eMMC5.1 JEDEC standard

5.4 RPMB Throughput improve

[Table 11] Related parameter register in EXT_CSD : WR_REL_PARAM [166]

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit[4]: EN_RPMB_REL_WR(R)

0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).

0 x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame), or 8KB(Thirthy two 512B frames).

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