Haier e-MMC Module

4GB HIKL4G-SSEE

INTRODUCTION

HIKL4G-SSEE is 4GB density of e-MMC Module product housed in 153 ball BGA package. This unit is utilized advanced Haier NAND flash device(s) and controller chip assembled as Multi Chip Module. HIKL4G-SSEE has an industry standard MMC protocol for easy use.

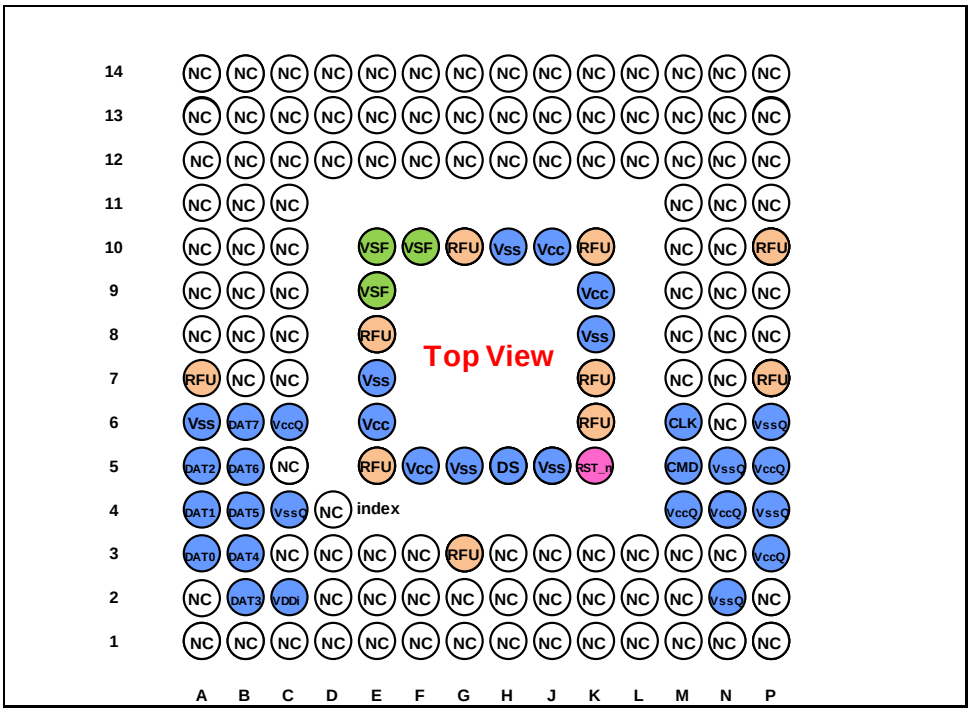
FEATURES

HIKL4G-SSEE Interface

HIKL4G-SSEE has the JEDEC/MMCA Version 5.0 interface with 1-I/O, 4-I/O and 8-I/O mode.

Pin Connection

P-WFBGA153-1113-0.50 (11.5mm x 13mm, H0.8mm max. package)



Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J5	Vss	N4	VccQ
A4	DAT1	C4	VssQ	J10	Vcc	N5	VssQ
A5	DAT2	C6	VccQ	K5	RST_n	P3	VccQ
A6	Vss	E6	Vcc	K8	Vss	P4	VssQ
B2	DAT3	E7	Vss	K9	Vcc	P5	VccQ
B3	DAT4	F5	Vcc	M4	VccQ	P6	VssQ
B4	DAT5	G5	Vss	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	Vss	N2	VssQ		

NC: No Connect, shall be connected to ground or left floating.
RFU: Reserved for Future Use, shall be left floating for future use.
VSF: Vendor Specific Function, shall be left floating.

Part Numbers

Available e-MMC Module Products – Part Numbers

Haier Part Number	Density	Package Size	NAND Flash Type	Weight
HIKL4G-SSEE	4GB	11.5mm x 13mm x 0.8mm(max)	1 x 32Gbit 15nm	0.18g typ

Operating Temperature

-25°C to +85°C

Storage Temperature

-40°C to +85°C

Performance

X8 mode/ Sequential access

Haier Part Number	Density	NAND Flash Type	Interleave Operation	Frequency /Mode	VccQ	Typ. Performance [MB/sec]	
						Read	Write
HIKL4G-SSEE	4GB	1 x 32Gbit 15nm	Non Interleave	52MHz/SDR	1.8V	46	14
					3.3V	46	14
				52MHz/DDR	1.8V	88	14
					3.3V	88	14
				HS200	1.8V	152	14
				HS400	1.8V	152	14

Power Supply

Vcc = 2.7V to 3.6V
VccQ = 1.7V to 1.95V / 2.7V to 3.6V

Operating Current (RMS)

The measurement for max RMS current is done as average RMS current consumption over a period of 100ms

Haier Part Number	Density	NAND Flash Type	Interleave Operation	Frequency /Mode	VccQ	Max Operating Current [mA]	
						Iccq	Icc
HIKL4G-SSEE	4GB	1 x 32Gbit 15nm	Non Interleave	52MHz/SDR	1.8V	60	25
					3.3V	70	25
				52MHz/DDR	1.8V	70	30
					3.3V	85	30
				HS200	1.8V	90	30
				HS400	1.8V	100	30

Sleep Mode Current

Haier Part Number	Density	NAND Flash Type	Interleave Operation	Iccqs [μA]		Iccqs+Iccs [μA]	
				Typ. *1	Max. *2	Typ. *1	Max. *2
HIKL4G-SSEE	4GB	1 x 32Gbit 15nm	Non Interleave	100	510	120	560

*1 : The conditions of typical values are 25°C and VccQ = 3.3V or 1.8V.
*2 : The conditions of maximum values are 85°C and VccQ = 3.6V or 1.95V.

Product Architecture

The diagram in Figure 1 illustrates the main functional blocks of the HIKL4G-SSEE Specification of the C_{REG} and recommended values of the C_{VCC}, and C_{VCCQ} in the Figure 1 are as follows.

Parameter	Symbol	Unit	Min.	Typ.	Max.	Remark
V_{DDi} capacitor value	C_{REG}	µF	0.10	-	2.2*	Except HS400
		µF	1.00	-	2.2*	HS400
V_{CC} capacitor value	C_{VCC}	µF	-	2.2 + 0.1	-	
V_{CCQ} capacitor value	C_{VCCQ}	µF	-	2.2 + 0.1	-	

* Haier recommends that the value should be usually applied as the value of C_{REG}.

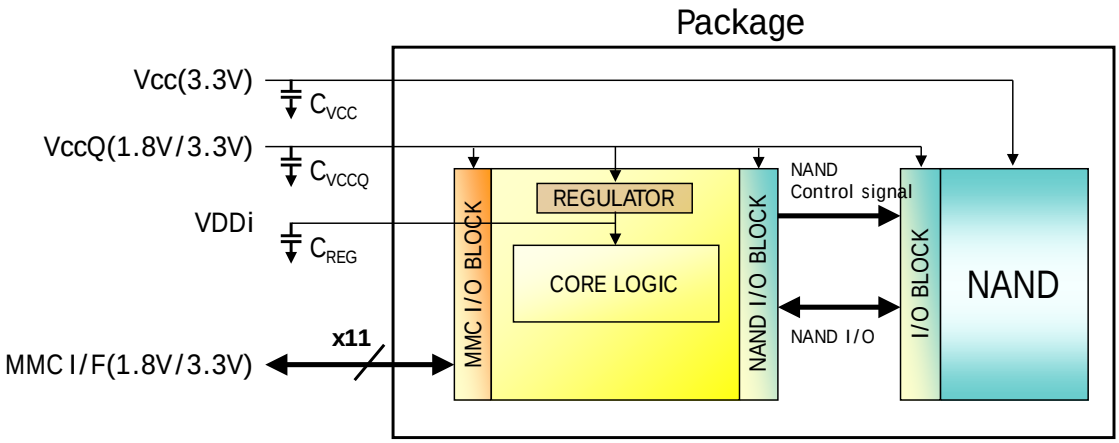


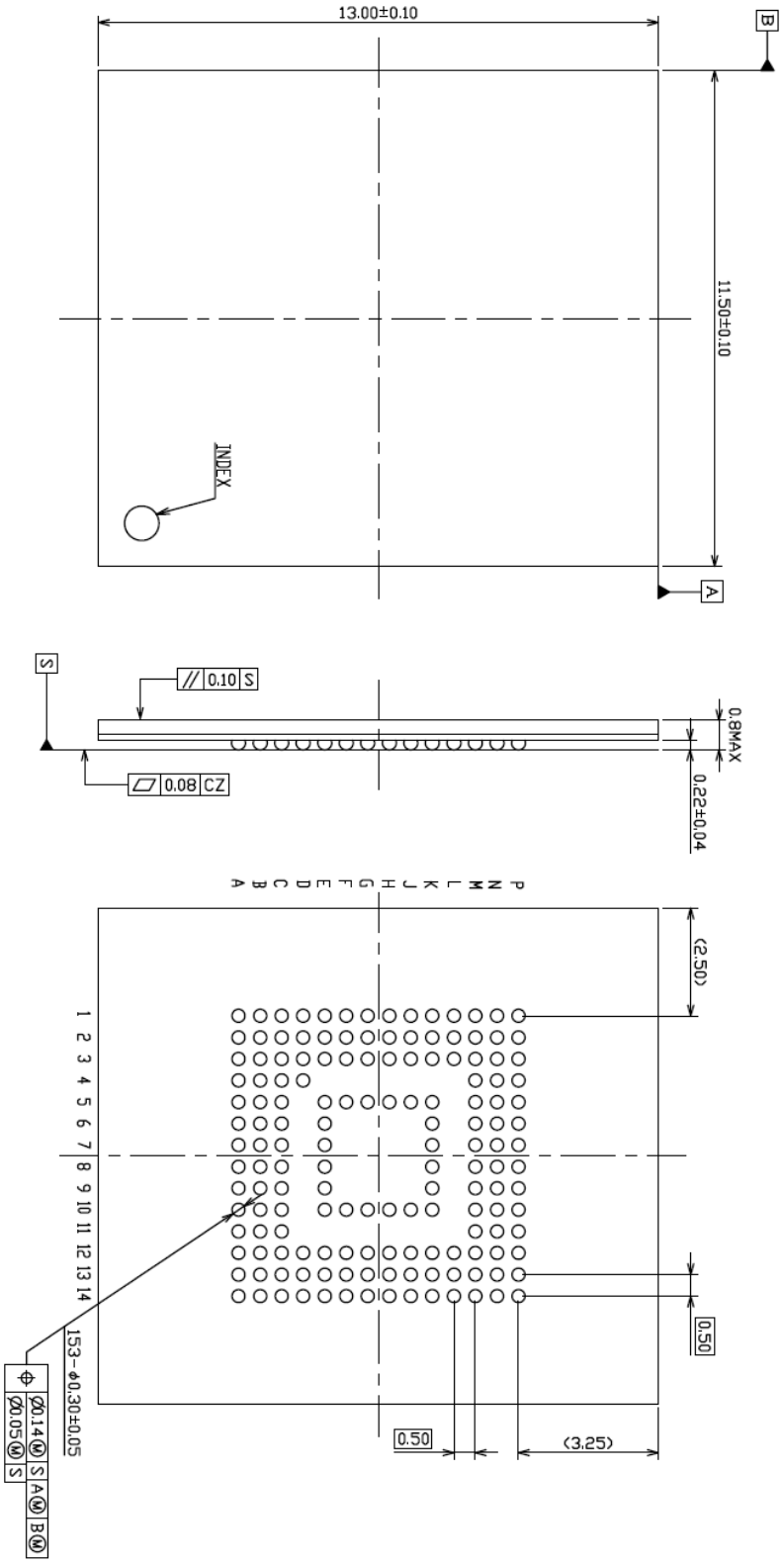
Figure 1 HIKL4G-SSEE Block Diagram

PRODUCT SPECIFICATIONS

Package Dimensions

P-WFBGA153-1113-0.50 (11.5mm x 13mm, H0.8mm max. package)

Unit: mm



Density Specifications

Density	Part Number	Interleave Operation	User Area Density [Bytes]	SEC_COUNT in Extended CSD
4GB	HIKL4G-SSEE	Non Interleave	3,959,422,976	0x00760000

1) User area density shall be reduced if enhanced user data area is defined.

Register Informations

OCR Register

OCR bit	VDD Voltage window	Value
[6:0]	Reserved	000 0000b
[7]	1.70-1.95 V	1b
[14:8]	2.0-2.6 V	000 0000b
[23:15]	2.7-3.6 V	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b
[31]	(card power up status bit (busy))[1]	

1) This bit is set to LOW if the Device has not finished the power up routine.

CID Register

CID-slice	Name	Field	Width	Value
[127:120]	Manufacturer ID	MID	8	0001 0001b
[119:114]	Reserved	-	6	0b
[113:112]	Device/BGA	CBX	2	01b
[111:104]	OEM/Application ID	OID	8	0b
[103:56]	Product name	PNM	48	0x30 30 34 47 41 30 (004GA0)
[55:48]	Product revision	PRV	8	0x02
[47:16]	Product serial	PSN	32	Serial number
[15:8]	Manufacturing date	MDT	8	see-JEDEC Specification
[7:1]	CRC7 checksum	CRC	7	CRC7
[0]	Not used, always ‘1’	-	1	1b

CSD Register

CSD-slice	Name	Field	Width	Cell Type	Value
[127:126]	CSD structure	CSD_STRUCTURE	2	R	0x3
[125:122]	System specification version	SPEC_VERS	4	R	0x4
[121:120]	Reserved	-	2	R	0x0
[119:112]	Data read access-time 1	TAAC	8	R	0x5E
[111:104]	Data read access-time 2 in CLK cycles (NSAC * 100)	NSAC	8	R	0x00
[103:96]	Max. bus clock frequency	TRAN_SPEED	8	R	0x32
[95:84]	Device command classes	CCC	12	R	0x0F5
[83:80]	Max. read data block length	READ_BL_LEN	4	R	0x9
[79:79]	Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0x0
[78:78]	Write block misalignment	WRITE_BLK_MISALIGN	1	R	0x0
[77:77]	Read block misalignment	READ_BLK_MISALIGN	1	R	0x0
[76:76]	DSR implemented	DSR_IMP	1	R	0x0
[75:74]	Reserved	-	2	R	0x0
[73:62]	Device size	C_SIZE	12	R	0xFFF
[61:59]	Max. read current @ VDD min.	VDD_R_CURR_MIN	3	R	0x7
[58:56]	Max. read current @ VDD max.	VDD_R_CURR_MAX	3	R	0x7
[55:53]	Max. write current @ VDD min.	VDD_W_CURR_MIN	3	R	0x7
[52:50]	Max. write current @ VDD max.	VDD_W_CURR_MAX	3	R	0x7
[49:47]	Device size multiplier	C_SIZE_MULT	3	R	0x7
[46:42]	Erase group size	ERASE_GRP_SIZE	5	R	0x1F
[41:37]	Erase group size multiplier	ERASE_GRP_MULT	5	R	0x1F
[36:32]	Write protect group size	WP_GRP_SIZE	5	R	0x07
[31:31]	Write protect group enable	WP_GRP_ENABLE	1	R	0x1
[30:29]	Manufacturer default ECC	DEFAULT_ECC	2	R	0x0
[28:26]	Write speed factor	R2W_FACTOR	3	R	0x4
[25:22]	Max. write data block length	WRITE_BL_LEN	4	R	0x9
[21:21]	Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0x0
[20:17]	Reserved	-	4	R	0x0
[16:16]	Content protection application	CONTENT_PROT_APP	1	R	0x0
[15:15]	File format group	FILE_FORMAT_GRP	1	R/W	0x0
[14:14]	Copy flag (OTP)	COPY	1	R/W	0x0
[13:13]	Permanent write protection	PERM_WRITE_PROTECT	1	R/W	0x0
[12:12]	Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	0x0
[11:10]	File format	FILE_FORMAT	2	R/W	0x0
[9:8]	ECC code	ECC	2	R/W/E	0x0
[7:1]	CRC	CRC	7	R/W/E	CRC
[0]	Not used, always ‘1’	-	1	-	0x1

Extended CSD Register

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[511:506]	Reserved	-	6	-	All '0'
[505]	Extended Security Commands Error	EXT_SECURITY_ERR	1	R	0x00
[504]	Supported Command Sets	S_CMD_SET	1	R	0x01
[503]	HPI features	HPI_FEATURES	1	R	0x01
[502]	Background operations support	BKOPS_SUPPORT	1	R	0x01
[501]	Max_packed read commands	MAX_PACKED_READS	1	R	0x3F
[500]	Max_packed write commands	MAX_PACKED_WRITES	1	R	0x3F
[499]	Data Tag Support	DATA_TAG_SUPPORT	1	R	0x01
[498]	Tag Unit Size	TAG_UNIT_SIZE	1	R	0x03
[497]	Tag Resource Size	TAG_RES_SIZE	1	R	0x00
[496]	Context management capabilities	CONTEXT_CAPABILITIES	1	R	0x7F
[495]	Large Unit size	LARGE_UNIT_SIZE_M1	1	R	0x00
[494]	Extended partitions attribute support	EXT_SUPPORT	1	R	0x03
[493]	Supported modes	SUPPORTED_MODES	1	R	0x01
[492]	FFU features	FFU_FEATURES	1	R	0x00
[491]	Operation codes timeout	OPERATION_CODES_TIMEOUT	1	R	0x00
[490:487]	FFU Argument	FFU_ARG	4	R	0xFFFFFFFF
[486]	Barrier support	BARRIER_SUPPORT	1	R	0x00
[485:309]	Reserved	-	177	-	All '0'
[308]	CMD Queuing Support	CMDQ_SUPPORT	1	R	0x00
[307]	CMD Queuing Depth	CMDQ_DEPTH	1	R	0x00
[306]	Reserved	-	1	-	0x00
[305:302]	Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	All '0'
[301:270]	Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	All '0'
[269]	Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	0x00
[268]	Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	0x01
[267]	Pre EOL information	PRE_EOL_INFO	1	R	0x01
[266]	Optimal read size	OPTIMAL_READ_SIZE	1	R	0x04
[265]	Optimal write size	OPTIMAL_WRITE_SIZE	1	R	0x04
[264]	Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	0x01
[263:262]	Device version	DEVICE_VERSION	2	R	0x00
[261:254]	Firmware version	FIRMWARE_VERSION	8	R	0x01
[253]	Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	0xAA
[252:249]	Cache size	CACHE_SIZE	4	R	0x00001000
[248]	Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	0x05
[247]	Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	0x32
[246]	Background operations status	BKOPS_STATUS	1	R	0x00
[245:242]	Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	0x00000000
[241]	1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	0x1E

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[240]	Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	0x00
[239]	Power class for 52MHz, DDR @ 3.6V	PWR_CL_DDR_52_360	1	R	0x22
[238]	Power class for 52MHz, DDR @ 1.95V	PWR_CL_DDR_52_195	1	R	0x77
[237]	Power class for 200MHz, @ VCCQ =1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	0x88
[236]	Power class for 200MHz, @ VCCQ=1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	0x88
[235]	Minimum Write Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	0x00
[234]	Minimum Read Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	0x50
[233]	Reserved	-	1	-	0x00
[232]	TRIM Multiplier	TRIM_MULT	1	R	0x01
[231]	Secure Feature support	SEC_FEATURE_SUPPORT	1	R	0x55
[230]	Secure Erase Multiplier	SEC_ERASE_MULT	1	R	0XDC
[229]	Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	0xFF
[228]	Boot information	BOOT_INFO	1	R	0x07
[227]	Reserved	-	1	R	0x00
[226]	Boot partition size	BOOT_SIZE_MULTI	1	R	0x10
[225]	Access size	ACC_SIZE	1	R	0x08
[224]	High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	0x08
[223]	High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	0x07
[222]	Reliable write sector count	REL_WR_SEC_C	1	R	0x01
[221]	High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	0x01
[220]	Sleep current (Vcc)	S_C_VCC	1	R	0x06
[219]	Sleep current (VccQ)	S_C_VCCQ	1	R	0x0A
[218]	Production state awareness timeout	PRODUCTION_STATE _AWARENESS_TIMEOUT	1	R	0x0A
[217]	Sleep/awake timeout	S_A_TIMEOUT	1	R	0x10
[216]	Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	0x10
[215:212]	Sector Count	SEC_COUNT 4GB	4	R	0x00760000
[211]	Secure Write Protection Information	SECURE_WP_INFO	1	R	0x00
[210]	Minimum Write Performance for 8bit @ 52MHz	MIN_PERF_W_8_52	1	R	0x00
[209]	Minimum Read Performance 8bit @ 52MHz	MIN_PERF_R_8_52	1	R	0x64
[208]	Minimum Write Performance for 8bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0x00
[207]	Minimum Read Performance for 8 bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	0x3C
[206]	Minimum Write Performance for 4bit @ 26MHz	MIN_PERF_W_4_26	1	R	0x00
[205]	Minimum Read Performance for 4bit @ 26MHz	MIN_PERF_R_4_26	1	R	0x1E

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[204]	Reserved	-	1	-	0x00
[203]	Power class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	0x22
[202]	Power class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	0x22
[201]	Power class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	0x66
[200]	Power class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	0x66
[199]	Partition switching timing	PARTITION_SWITCH_TIME	1	R	0x01
[198]	Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	0x0A
[197]	I/O Driver Strength	DRIVER_STRENGTH	1	R	0x1F
[196]	Device Type	DEVICE_TYPE	1	R	0x57
[195]	Reserved	-	1	-	0x00
[194]	CSD structure	CSD_STRUCTURE	1	R	0x02
[193]	Reserved	-	1	-	0x00
[192]	Extended CSD revision	EXT_CSD_REV	1	R	0x07
[191]	Command Set	CMD_SET	1	R/W/E_P	0x00
[190]	Reserved	-	1	-	0x00
[189]	Command set revision	CMD_SET_REV	1	R	0x00
[188]	Reserved	-	1	-	0x00
[187]	Power class [1]	POWER_CLASS	1	R/W/E_P	0x00
[186]	Reserved	-	1	-	0x00
[185]	High-speed interface timing	HS_TIMING	1	R/W/E_P	0x00
[184]	Strobe Support	STROBE_SUPPORT	1	R	0x00
[183]	Bus width mode	BUS_WIDTH	1	W/E_P	0x00
[182]	Reserved	-	1	-	0x00
[181]	Erased memory content	ERASED_MEM_CONT	1	R	0x00
[180]	Reserved	-	1	-	0x00
[179]	Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	0x00
[178]	Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	0x00
[177]	Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	0x00
[176]	Reserved	-	1	-	0x00
[175]	High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	0x00
[174]	Boot write protection status registers	BOOT_WP_STATUS	1	R	0x00
[173]	Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	0x00
[172]	Reserved	-	1	-	0x00
[171]	User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	0x00
[170]	Reserved	-	1	-	0x00
[169]	FW configuration	FW_CONFIG	1	R/W	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[168]	RPMB Size	RPMB_SIZE_MULT	1	R	0x04
[167]	Write reliability setting register	WR_REL_SET	1	R/W	0x1F
[166]	Write reliability parameter register	WR_REL_PARAM	1	R	0x05
[165]	Start Sanitize operation	SANITIZE_START	1	W/E_P	0x00
[164]	Manually start background operations	BKOPS_START	1	W/E_P	0x00
[163]	Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	0x00
[162]	H/W reset function	RST_n_FUNCTION	1	R/W	0x00
[161]	HPI management	HPI_MGMT	1	R/W/E_P	0x00
[160]	Partitioning Support	PARTITIONING_SUPPORT	1	R	0x07
[159:157]	Max Enhanced Area Size [2]	MAX_ENH_SIZE_MULT	3	R	0x0001D8
[156]	Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	0x00
[155]	Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	0x00
[154:143]	General Purpose Partition Size [3]	GP_SIZE_MULT	12	R/W	0x00
[142:140]	Enhanced User Data Area Size [4]	ENH_SIZE_MULT	3	R/W	0x00
[139:136]	Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	0x00
[135]	Reserved	-	1	-	0x00
[134]	Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	0x00
[133]	Production state awareness[5]	PRODUCTION_STATE_AWARENESS	1	R/W/E	0x00
[132]	Package Case Temperature is controlled[1]	TCASE_SUPPORT	1	W/E_P	0x00
[131]	Periodic Wake-up[1]	PERIODIC_WAKEUP	1	R/W/E	0x00
[130]	Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	0x01
[129:128]	Reserved	-	2	-	All '0'
[127:64]	Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	-	-
[63]	Native sector size	NATIVE_SECTOR_SIZE	1	R	0x01
[62]	Sector size emulation	USE_NATIVE_SECTOR	1	R/W	0x00
[61]	Sector size	DATA_SECTOR_SIZE	1	R	0x00
[60]	1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	0x0A
[59]	Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	0x00
[58]	Number of addressed group to be Released	DYNCAP_NEEDED	1	R	0x00
[57:56]	Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	0x0000
[55:54]	Exception events status	EXCEPTION_EVENTS_STATUS	2	R	0x0000
[53:52]	Extended partitions attribute[1]	EXT_PARTITIONS_ATTRIBUTE	2	R/W	0x0000
[51:37]	Context configuration	CONTEXT_CONF	15	R/W/E_P	0x00
[36]	Packed command status	PACKED_COMMAND_STATUS	1	R	0x00
[35]	Packed command failure index	PACKED_FAILURE_INDEX	1	R	0x00
[34]	Power Off Notification[5]	POWER_OFF_NOTIFICATION	1	R/W/E_P	0x00
[33]	Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[32]	Flushing of the cache	FLUSH_CACHE	1	W/E_P	0x00
[31]	Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	0x00
[30]	Mode config	MODE_CONFIG	1	R/W/E_P	0x00
[29]	Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	0x00
[28:27]	Reserved	-	2	-	All '0'
[26]	FFU status	FFU_STATUS	1	R	0x00
[25:22]	Pre loading data size[6]	PRE_LOADING_DATA_SIZE	4	R/W/E_P	0x00760000
[21:18]	Max pre loading data size	MAX_PRE_LOADING DATA _SIZE 4GB	4	R	0x00760000
[17]	Product state awareness enablement[5]	PRODUCT_STATE _AWARENESS_ENABLEMENT	1	R/W/E &R	0x03
[16]	Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	0x09
[15]	Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	0x00
[14:0]	Reserved	-	15	-	All '0'

[1] Although these fields can be re-written by host, Haier e-MMC does not support.

[2] Max Enhanced Area Size (MAX_ENH_SIZE_MULT [159:157]) has to be calculated by following formula.

Max Enhanced Area = MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes

$$\sum_{i=1}^{4} \text{Enhanced general partition size}(i) + \text{Enhanced user data area} \le \text{Max enhanced area}$$

[3] General Purpose Partition Size (GP_SIZE_MULT_GP0 - GP_SIZE_MULT_GP3 [154:143]) has to be calculated by following formula.

General_Purpose_Partition_X Size = (GP_SIZE_MULT_X_2 x 2^{16} + GP_SIZE_MULT_X_1 x 2^{8}
+ GP_SIZE_MULT_X_0 x 2^{0}) x HC_WP_GRP_SIZE
x HC_ERASE_GRP_SIZE x 512kBytes

[4] Enhanced User Data Area Size (ENH_SIZE_MULT [142:140]) has to be calculated by following formula.

Enhanced User Data Area x Size = (ENH_SIZE_MULT_2 x 2^{16} + ENH_SIZE_MULT_1 x 2^{8}
+ ENH_SIZE_MULT_0 x 2^{0}) x HC_WP_GRP_SIZE
x HC_ERASE_GRP_SIZE x 512kBytes

[5] Haier recommends to issue the Power Off Notification before turning off the device, especially when cache is on or AUTO_EN(BKOPS_EN[163]:bit1) is set to '1b'.

[6] - Pre loading data size = PRE_LOADING_DATA_SIZE x Sector Size
Pre-loading data size should be multiple of 4KB and the pre-loading data should be written by multiple of 4KB chunk size, aligned with 4KB address. This is because the valid data size will be treated as 4KB when host writes data less than 4KB.

- If the host continues to write data in Normal state (after it wrote PRE_LOADING_DATA_SIZE amount of data) and before soldering, the pre-loading data might be corrupted after soldering.

- If a power cycle is occurred during the data transfer, the amount of data written to device is not clear. Therefore in this case, host should erase the entire pre-loaded data and set again PRE_LOADING_DATA_SIZE[25:22], PRODUCTION_STATE_AWARENESS[133], and PRODUCT_STATE_AWARENESS_ENABLEMENT[17].