Haier

Data Sheet - Confidential

iNAND® *7250*

e.MMC 5.1 with HS400 Interface

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REVISION HISTORY

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1. INTRODUCTION

1.1. General Description

Overview Haier iNAND 7250 is an Embedded Flash Drive (EFD) designed for write intensive applications in a wide range of home entertainment and security applications, such as Set-Top-Box (STB), Over The Top (OTT), Home Gateways, Smart TV, Smart Security Cameras and more. The iNAND 7250 utilizes an LDPC ECC machine and MLC memory to provide a robust, high performance, high quality and high endurance product. The LDPC engine significantly improves error correction enabling longer device lifetime and an increased ability to handle operation at high temperature.

The iNAND 7250 provides 8GB to 64GB of capacity and supports e.MMC 5.1. The iNAND 7250 is the ideal choice to deliver high reliability and high performance for storage applications like imaging, video, music, GPS, gaming, email, office and other new applications such as NOR replacement for embedded systems or other devices.

The design of the iNAND 7250 is based on a JEDEC compatible form factor measuring 11.5x13mm (153 balls) for all capacities to lower integration costs and accelerate time-to-market.

Architecture iNAND 7250 combines an embedded thin flash controller with advanced enterprise Multi-level Cell (eMLC) NAND flash technology enhanced by Haier embedded flash management software running as firmware on the flash controller. iNAND 7250 employs an industry-standard eMMC 5.1[1] interface featuring Command-Queue, HS400 interface, FFU, as well as legacy eMMC 4.51 features such as EUDA, Power Off Notifications, Packed commands, Cache, Boot / RPMB partitions, HPI, and HW Reset, making it an optimal device for both reliable code and data storage.

Like our other iNAND products, iNAND 7250 offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as an advanced power management scheme.

iNAND 7250 architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, Haier firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximizing flash life expectancy.

iNAND 7250 also includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

Combining high performance with features for easy integration and exceptional reliability, iNAND 7250 is an EFD designed to exceed the demands of both manufacturers and their customers.

[1] Compatible to JESD84-B51

1.2. Plug-and-Play Integration

iNAND's optimized architecture eliminates the need for complicated software integration and testing processes thereby enabling plug-and-play integration into the host system. The replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This allows manufacturers to adopt advanced NAND Flash technologies and update product lines with minimal integration or qualification efforts.

iNAND 7250 features a MMC interface allows for easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the Haier iNAND 7250 with MMC Interface.

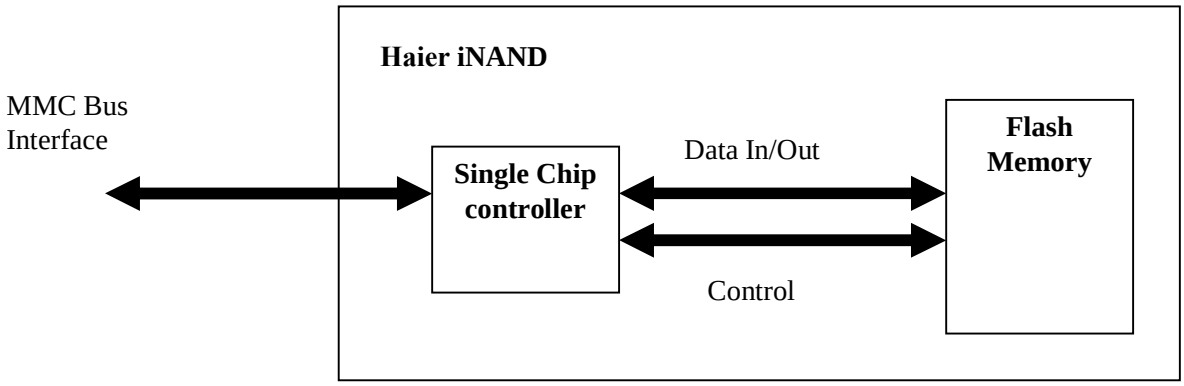

Figure 1 - Haier iNAND 7250 with MMC Interface Block Diagram

1.3. Feature Overview

Haier iNAND 7250, with MMC interface, includes the following features:

- Memory controller and NAND flash
- Mechanical design that complies with JEDEC Specifications with specific optimizations for automotive applications
- Offered in three TFBGA packages of e.MMC 5.1
  - 11.5mm x 13mm x 0.8mm (8GB-16GB)
  - 11.5mm x 13mm x 1.0mm (32GB)
  - 11.5mm x 13mm x 1.2mm (64GB)
- Operating temperature range: –25C° to +85C°
- Dual power system
  - Core voltage (VCC) 2.7-3.6 V
  - I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
- 8GB - 64GB of data storage
- Supports three data bus widths: 1bit (default), 4bit, 8bit
- Complies with e.MMC Specification Ver. 5.1 HS400
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Up to 300 MB/sec bus transfer rate, using 8 parallel data lines at 200 MHz, HS400 Mode
- High data integrity with eMLC memory, advanced LDPC ECC engine, automatic refresh, advanced power protection
- Flexible EUDA, Fast boot
- Up to 3K P/E cycles, 10 year data retention @ 55°C fresh

1.4. MMC bus and Power Lines

Haier iNAND 7250 supports the MMC interface protocol. For more details regarding these buses refer to JEDEC standard No. JESD84-B51.

The iNAND bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input.
- VCCQ: Power supply line for host interface.
- VCC: Power supply line for internal flash memory.
- VDDi: iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: Ground lines.
- RCLK: Data strobe.
- VSF: Vendor specific functions used for debugging purposes.

1.4.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

2. E.MMC SELECTED FEATURES OVERVIEW

iNAND 7250 supported features list:

Table 3 – Proprietary Features list

e.MMC	Device Features	Benefit	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Max theoretical Speed	Up to 400MB/s
4.41	EUDA	Enhanced User Data Area for higher endurance	Yes
4.41	SECURE ERASE/TRIM	“True Wipe”	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	Yes
4.41	PARTITIONING & PROTECTION	Flexibility	Yes
4.41	BACKGROUND OPERATIONS	Better User Experience (low latency)	Yes
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	Yes
4.41	HARDWARE RESET	Robust System Design	Yes
4.41	HPI	Control Long Reads/Writes	Yes
4.41	RPMB	Secure Folders	Yes
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	Yes
4.5	LARGE SECTOR SIZE	Potential performance	No
4.5	SANITIZE (4.51)	“True Wipe”	Yes
4.5	PACKED COMMANDS	Reduce Host Overhead	Yes
4.5	DISCARD	Improved Performance on Full Media	Yes
4.5	DATA TAG	Performance and/or Reliability	Yes (API only)
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	Yes (API only)
4.5	CACHE	Better Sequential & Random Writes	Yes
5.0	SECURED FIELD FIRMWARE UPGRADE (sFFU)	Enables feature enhancements in the field	Yes
5.0	PRODUCTION STATE AWARENESS	Different operation during production	Yes
5.0	DEVICE HEALTH	Vital NAND info	Yes
5.1	ENHANCE STROBE	Sync between Device and Host in HS400	Yes
5.1	COMMAND QUEUE	Responsiveness	Yes
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	Yes
5.1	CACHE FLUSH AND BARRIER	Ordered Cache flushing	Yes
5.1	BKOPS CONTROLLER	Host control on BKOPs	Yes
5.1	SECURE WP	Secure Write Protect	Yes
5.1	PRE EOL	Pre End Of Life notification	Yes
Proprietary	VSF	Enable on-board debugging	Yes
Proprietary	PNM	Special product name	Yes
Proprietary	DEVICE REPORT	Device Firmware status	Yes

2.1. HS400 Interface

Haier 7250 supports HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 4 or 8 bit bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data. For additional information please refer to JESD84-B51 standard.

2.2. Enhanced User Data Area (EUDA)

For write intensive applications, there is a need for an area of higher endurance or performance. To address this, Haier 7250 allows for the definition of an enhanced user data area as specified in the JESD84-B51 standard. This area is a true SLC partition. The EUDA is a designated area of the general User Data Area. The configuration is one-time programmable.

2.3. Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the e.MMC device and instructs the e.MMC device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user/OS data. During the FFU process, the host can replace firmware files or single/all file systems.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the Haier lab
2. The sFFU files are handed to Haier customer
3. Haier customer can push the firmware updates to their end-users in a transparent way

Note 1: The sFFU process and sFFU files are protected against leakage to unauthorized entities.

Note 2: During the sFFU process the Host may retrieve the exact status of the process using the smart report feature.

For additional information please refer to JESD84-B51 standard and the Haier application note on this subject.

2.4. Cache

The eMMC cache is dedicated volatile memory at the size of 512KB. Caching enables to improve iNAND performance for both sequential and random access. For additional information please refer to JESD84-B51 standard.

2.5. Discard

iNAND supports discard command as defined in e.MMC 5.1 spec. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

2.6. Power off Notifications

iNAND supports power off notifications as defined in e.MMC 5.1 spec. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

2.7. Packed Commands

To enable optimal system performance, iNAND supports packed commands as defined in e.MMC 5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

2.8. Boot Partition

iNAND supports e.MMC 5.1 boot operation mode: factory configuration supplies two boot partitions each 4MB in size for 8GB-64GB.

2.9. RPMB Partition

iNAND supports e.MMC 5.1 RPMB operation mode: factory configuration supplies one RPMB partition 4MB in size for 8GB-64GB.

2.10. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.11. Sleep (CMD5)

An iNAND 7250 device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer to JESD84-B51.

2.12. Enhanced Reliable Write

iNAND 7250 supports enhanced reliable write as defined in e.MMC 5.1 spec.

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.13. Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

2.14. Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND 7250 supports the optional Secure Erase command.

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

2.15. Secure Trim

For backward compatibility reasons, iNAND 7250 support Secure Trim command. The Secure Trim5 command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

The secure trim command is performed in two steps:

1) Mark the LBA range as candidate for erase.
2) Erase the marked address range and ensure no old copies are left.

2.16. Partition Management

iNAND 7250 offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows

Factory configuration supplies two boot partitions (refer to section 2.8) implemented as enhanced storage media and one RPMB partitioning of 4MB in size (refer to section 2.9).

Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

2.17. Device Health

Device Health is similar to SMART features of modern hard disks, it provides only vital NAND flash program/erase cycles information in percentage of useful flash life span.

The host can query Device Health information utilizing standard MMC command, to get the extended CSD structure:

- DEVICE_LIFE_TIME_EST_TYP_A[268], the host may use it to query SLC device health information
- DEVICE_LIFE_TIME_EST_TYP_B[269], the host may use it to query MLC device health information

The device health feature will provide a % of the wear of the device in 10% fragments.

2.18. EOL Status

EOL status is implemented according to the eMMC 5.1 spec. One additional state (state 4) was added to INAND 7250 which indicates that the device is in EOL mode.

2.19. Enhanced Write Protection

To allow the host to protect data against erase or write iNAND 7250 supports two levels of write protect command.

The entire iNAND 7250 (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD Specific segments of iNAND 7250 may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

For additional information please refer to the JESD84-B51 standard.

2.20. High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in JESD84-B51 enables low read latency operation by suspending a lower priority operation before it is actually completed.

For additional information on the HPI function, refer to JESD84-B51.

2.21. H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B51 standard.

2.22. Host-Device Synchronization Flow (Enhanced STROBE)

The Enhanced STROBE feature as implemented in iNAND 7250 allows utilizing STROBE to synchronize also the CMD response:

- CMD clocking stays SDR (similar to legacy DDR52)
- Host commands are clocked out with the rising edge of the host clock (as done in legacy eMMC devices)
- iNAND 7250 will provide STROBE signaling synced with the CMD response in addition to DATA Out
- Host may use the STROBE signaling for DAT and CMD-Response capturing eliminating the need for a tuning mechanism

This feature requires support by the host to enable faster and more reliable operation.

2.23. Command-Queue

e.MMC Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash